



144 pin SO-DIMM SDRAM Modules

HYS64V16200GDL
HYS64V32220GDL

128MB & 256 MB PC100 / PC133

- 144 Pin Eight Byte Small Outline Dual-In-Line Synchronous DRAM Modules for PC100 and PC133 notebook applications
- One bank 16M x 64 (128MByte) and two banks 32M x 64 (256 MByte) non-parity module organisation
- Performance:

| | | -7 | -7.5 | -8 | |
|-----------------|------------------------|----------------|----------------|----------------|-------|
| | | PC133 2-2-2 | PC133 3-3-3 | PC100 2-2-2 | Units |
| f _{CK} | Clock frequency (max.) | 133 | 133 | 100 | MHz |
| t _{AC} | Clock access time | 5.4 | 5.4 | 6 | ns |

- Single +3.3V(± 0.3V) power supply
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTTL compatible
- Serial Presence Detect with E²PROM
- 256Mbit SDRAM low power components in TSOP54 packages with 16M x 16 organisation
- 8192 refresh cycles every 64 ms
- Gold contact pad, JEDEC MO-190 outline dimensions
- This module family is fully compliant with the latest INTEL SO-DIMM layout and electrical specifications
- All PC133 modules are fully backward compatible to PC100-222 operation
- **Importante Notice:**
These SO-DIMM modules are based on 256Mbit SDRAM technology and can be used in applications only, where 256Mbit addressing is supported.

This INFINEON modules are industry standard 144 pin 8-byte Synchronous DRAM (SDRAM) Small Outline Dual In-line Memory Modules (SO-DIMM) which are organised as x64 high speed memory arrays designed for use in non-parity applications. These SO-DIMMs use 256Mbit SDRAMs in TSOPII packages. Decoupling capacitors are mounted on the board.

The DIMMs use serial presence detects implemented via a serial E²PROM using the two pin I²C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All INFINEON 144-pin SO-DIMMs provide a high performance, flexible 8-byte interface in a 67,6 mm long footprint.

Product Spectrum:

| | | Speed | SDRAMs used | RowAddr. | Bank Select | Column Addr. | Refresh Period |
|----------|--------------------|-----------|-------------|----------|-------------|--------------|----------------|
| 16M x 64 | HYS64V16200GDL-7 | PC133-222 | 4 16Mx16 | 13 | BA0, BA1 | 9 | 8k |
| | HYS64V16200GDL-7.5 | PC133-333 | | | | | |
| | HYS64V16200GDL-8 | PC100-222 | | | | | |
| 32M x 64 | HYS64V32220GDL-7 | PC133-222 | 8 16Mx16 | | | | 7,8 μs |
| | HYS64V32220GDL-7.5 | PC133-333 | | | | | |
| | HYS64V32220GDL-8 | PC100-222 | | | | | |

Note: All partnumbers end with a place code, designating the die revision. Example: HYS64V32220GDL-8-C2, indicating Rev.C2 dies are used for SDRAM components.

Card Dimensions:

| Organisation | PCB-Board | L x H x T [mm] |
|--------------|--------------------|----------------------|
| 16M x 64 | INTEL Rev. 1.0/1.2 | 67.60 x 25.40 x 3.80 |
| 32M x 64 | | 67.60 x 31.75 x 3.80 |

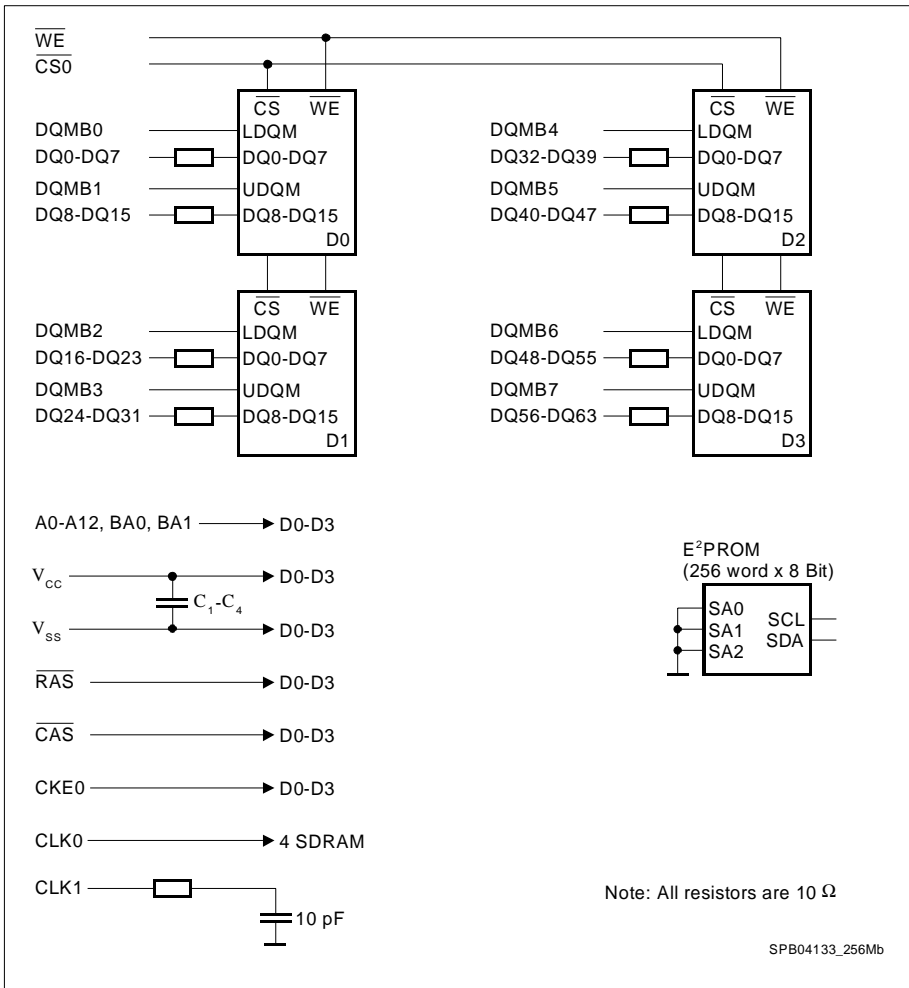
Pin Names

| | | | |
|------------------|-----------------------|--|-------------------------------------|
| A0-A12 | Address Inputs | DQMB0 -DQMB7 | Data Mask |
| BA0,BA1 | Bank Selects | $\overline{CS0}$, $\overline{CS1}$ *) | Chip Select |
| DQ0 - DQ63 | Data Input/Output | Vcc | Power (+3.3 Volt) |
| \overline{RAS} | Row Address Strobe | Vss | Ground |
| \overline{CAS} | Column Address Strobe | SCL | Clock for Presence Detect |
| \overline{WE} | Read / Write Input | SDA | Serial Data Out for Presence Detect |
| CKE0, CKE1 | Clock Enable | N.C. | No Connection |
| CLK0, CLK1 *) | Clock Input | | |

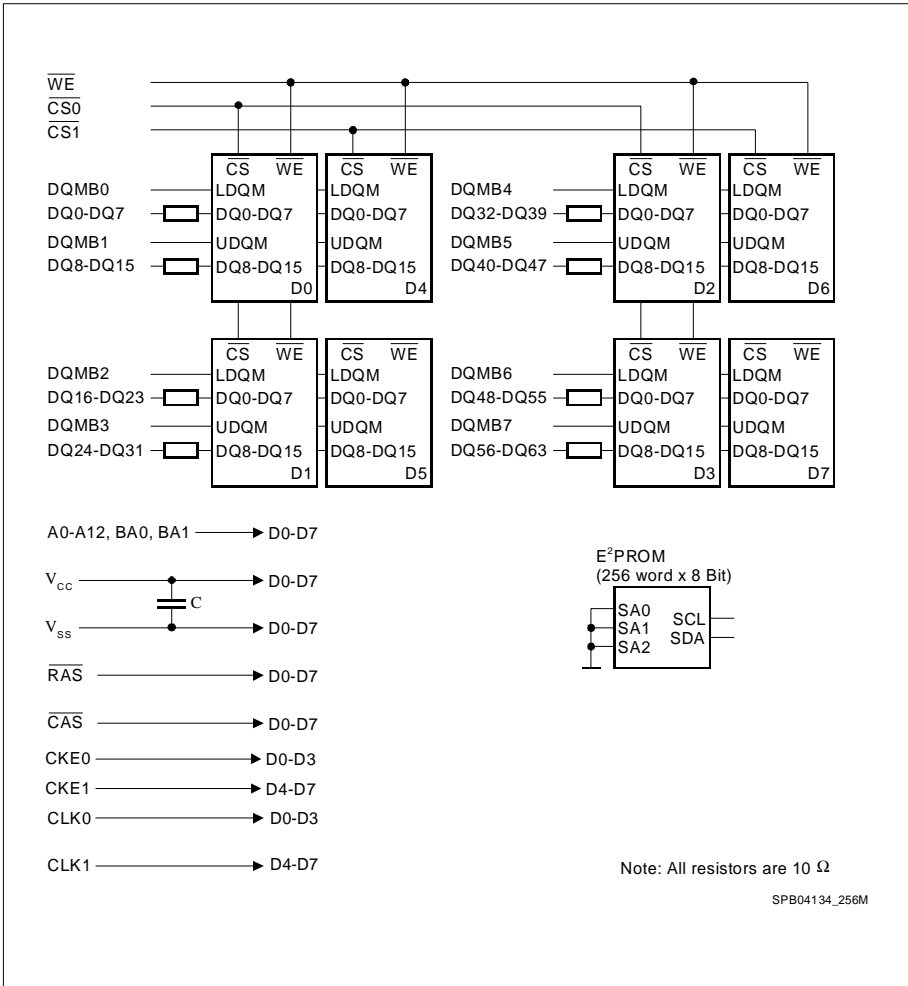
*) $\overline{CS1}$ and CKE1 on two bank modules only

Pin Configuration

| PIN # | Front Side | PIN # | Back Side | PIN # | Front Side | PIN # | Back Side |
|-------|------------|-------|-----------|-------|------------|-------|-----------|
| 1 | VSS | 2 | VSS | 73 | NC | 74 | CLK1 |
| 3 | DQ0 | 4 | DQ32 | 75 | Vss | 76 | Vss |
| 5 | DQ1 | 6 | DQ33 | 77 | NC | 78 | NC |
| 7 | DQ2 | 8 | DQ34 | 79 | NC | 80 | NC |
| 9 | DQ3 | 10 | DQ35 | 81 | Vcc | 82 | Vcc |
| 11 | VCC | 12 | Vcc | 83 | DQ16 | 84 | DQ48 |
| 13 | DQ4 | 14 | DQ36 | 85 | DQ17 | 86 | DQ49 |
| 15 | DQ5 | 16 | DQ37 | 87 | DQ18 | 88 | DQ50 |
| 17 | DQ6 | 18 | DQ38 | 89 | DQ19 | 90 | DQ51 |
| 19 | DQ7 | 20 | DQ39 | 91 | Vss | 92 | Vss |
| 21 | Vss | 22 | Vss | 93 | DQ20 | 94 | DQ52 |
| 23 | DQMB0 | 24 | DQMB4 | 95 | DQ21 | 96 | DQ53 |
| 25 | DQMB1 | 26 | DQMB5 | 97 | DQ22 | 98 | DQ54 |
| 27 | Vcc | 28 | Vcc | 99 | DQ23 | 100 | DQ55 |
| 29 | A0 | 30 | A3 | 101 | Vcc | 102 | Vcc |
| 31 | A1 | 32 | A4 | 103 | A6 | 104 | A7 |
| 33 | A2 | 34 | A5 | 105 | A8 | 106 | BA0 |
| 35 | Vss | 36 | Vss | 107 | Vss | 108 | Vss |
| 37 | DQ8 | 38 | DQ40 | 109 | A9 | 110 | BA1 |
| 39 | DQ9 | 40 | DQ41 | 111 | A10 | 112 | A11 |
| 41 | DQ10 | 42 | DQ42 | 113 | Vcc | 114 | Vcc |
| 43 | DQ11 | 44 | DQ43 | 115 | DQMB2 | 116 | DQMB6 |
| 45 | Vcc | 46 | Vcc | 117 | DQMB3 | 118 | DQMB7 |
| 47 | DQ12 | 48 | DQ44 | 119 | Vss | 120 | Vss |
| 49 | DQ13 | 50 | DQ45 | 121 | DQ24 | 122 | DQ56 |
| 51 | DQ14 | 52 | DQ46 | 123 | DQ25 | 124 | DQ57 |
| 53 | DQ15 | 54 | DQ47 | 125 | DQ26 | 126 | DQ58 |
| 55 | Vss | 56 | Vss | 127 | DQ27 | 128 | DQ59 |
| 57 | NC | 58 | NC | 129 | Vcc | 130 | Vcc |
| 59 | NC | 60 | NC | 131 | DQ28 | 132 | DQ60 |
| 61 | CLK0 | 62 | CKE0 | 133 | DQ29 | 134 | DQ61 |
| 63 | Vcc | 64 | Vcc | 135 | DQ30 | 136 | DQ62 |
| 65 | RAS | 66 | CAS | 137 | DQ31 | 138 | DQ63 |
| 67 | WE | 68 | CKE1 | 139 | Vss | 140 | Vss |
| 69 | CS0 | 70 | A12 | 141 | SDA | 142 | SCL |
| 71 | CS1 | 72 | N.C | 143 | Vcc | 144 | Vcc |



Block Diagram for one bank 16M x 64 (128MByte) SDRAM SO- DIMM - Module



Block Diagram for two bank 32M x 64 (256MByte) SDRAM SO-DIMM - Module

Absolute Maximum Ratings

| Parameter | Symbol | Limit Values | | Unit |
|---|-------------------|--------------|------|------|
| | | min. | max. | |
| Input / Output voltage relative to V_{SS} | V_{IN}, V_{OUT} | - 1.0 | 4.6 | V |
| Power supply voltage on V_{DD} | V_{DD} | - 1.0 | 4.6 | V |
| Storage temperature range | T_{STG} | -55 | +150 | °C |
| Power dissipation (per SDRAM component) | P_D | - | 1 | W |
| Data out current (short circuit) | I_{OS} | - | 50 | mA |

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded.
 Functional operation should be restricted to recommended operation conditions.
 Exposure to higher than recommended voltage for extended periods of time affect device reliability

DC Characteristics

$T_A = 0$ to 70 °C; $V_{SS} = 0$ V; $V_{DD} = 3.3$ V \pm 0.3 V

| Parameter | Symbol | Limit Values | | Unit |
|---|------------|--------------|--------------|------|
| | | min. | max. | |
| Input high voltage | V_{IH} | 2.0 | $V_{CC}+0.3$ | V |
| Input low voltage | V_{IL} | - 0.5 | 0.8 | V |
| Output high voltage ($I_{OUT} = -4.0$ mA) | V_{OH} | 2.4 | - | V |
| Output low voltage ($I_{OUT} = 4.0$ mA) | V_{OL} | - | 0.4 | V |
| Input leakage current, any input (0 V < $V_{IN} < 3.6$ V, all other inputs = 0 V) | $I_{I(L)}$ | - 20 | 20 | mA |
| Output leakage current (DQ is disabled, 0 V < $V_{OUT} < V_{DD}$) | $I_{O(L)}$ | - 20 | 20 | mA |

Capacitance

$T_A = 0$ to 70 °C; $V_{DD} = 3.3$ V \pm 0.3 V, $f = 1$ MHz

| Parameter | Symbol | Limit Values | | Unit |
|---|----------|---------------|---------------|------|
| | | 16M x 64 max. | 32M x 64 max. | |
| Input capacitance (A0 to A11, BA0, BA1) | C_{I1} | 28 | 52 | pF |
| Input capacitance (\overline{RAS} , \overline{CAS} , \overline{WE} , $\overline{CKE0}$) | C_{I2} | 25 | 46 | pF |
| Input Capacitance (CLK0, CLK1) | C_{I3} | 35 | 35 | pF |
| Input capacitance (CS0) | C_{I4} | 25 | 30 | pF |
| Input capacitance (DQMB0-DQMB7) | C_{I5} | 10 | 15 | pF |
| Input / Output capacitance (DQ0-DQ63) | C_{IO} | 12 | 18 | pF |
| Input Capacitance (SCL, SA0-2) | C_{sc} | 8 | 8 | pF |
| Input/Output Capacitance | C_{sd} | 10 | 10 | pF |

Operating Currents per memory bank

(TA = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V)

(Recommended Operating Conditions unless otherwise noted)

| Parameter & Test Condition | | Symb. | -7/-7.5 | -8 | | Note |
|--|--|-------------------------|---------|-----|----|------|
| OPERATING CURRENT | | | | | | |
| trc=trcmin., All banks operated in random access, all banks operated in ping-pong manner | | ICC1 | 920 | 680 | mA | 1, 2 |
| PRECHARGE STANDBY CURRENT in Power Down Mode CS = VIH (min.), CKE<=Vil(max) | | tck = min. ICC2P | 8 | | mA | 1 |
| PRECHARGE STANDBY CURRENT in Non-Power Down Mode CS = VIH (min.), CKE>=Vih(min) | | tck = min. ICC2N | 160 | 120 | mA | 1 |
| NO OPERATING CURRENT tck = min., CS = VIH(min), active state (max. 4 banks) | | CKE>=VIH(min.) ICC3N | 200 | 180 | mA | 1 |
| | | CKE<=VIL(max.) ICC3P | 40 | | mA | 1 |
| BURST OPERATING CURRENT tck = min., Read command cycling | | ICC4 | 600 | 400 | mA | 1,2 |
| AUTO REFRESH CURRENT tck = min., Auto Refresh command cycling | | ICC5 | 960 | 880 | mA | 1 |
| SELF REFRESH CURRENT Self Refresh Mode, CKE=0.2V, tck = infinity. | | ICC6 | 7.2 | | mA | 1 |

Notes:

1. These parameters depend on the cycle rate. These values are measured at 133 MHz for -7 & -7.5 and at 100 MHz for -8 modules. Input signals are changed once during tck.
2. These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the data-out current is excluded.

AC Characteristics 1)2)

(TA = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns)

| Parameter | Symbol | Limit Values | | | | | | Unit |
|-----------|--------|-----------------|------|-------------------|------|-----------------|------|------|
| | | -7 PC133-222 | | -7.5 PC133-333 | | -8 PC100-222 | | |
| | | min. | max. | min. | max. | min. | max. | |

Clock and Access Time

| | | | | | | | | | | |
|------------------------|----------|------------------------------|-----|-----|-----|-----|-----|-----|-----|---------|
| Clock Cycle Time | t_{CK} | \overline{CAS} Latency = 3 | 7.5 | – | 7.5 | – | 10 | – | ns | |
| | | \overline{CAS} Latency = 2 | 7.5 | – | 10 | – | 10 | – | ns | |
| Clock Frequency | t_{CK} | \overline{CAS} Latency = 3 | – | 133 | – | 133 | – | 100 | MHz | |
| | | \overline{CAS} Latency = 2 | – | 133 | – | 100 | – | 100 | MHz | |
| Access Time from Clock | t_{AC} | \overline{CAS} Latency = 3 | – | 5.4 | – | 5.4 | – | 6 | ns | 2, 3 |
| | | \overline{CAS} Latency = 2 | – | 5.4 | – | 6 | – | 6 | ns | |
| Clock High Pulse Width | t_{CH} | | 2.5 | – | 2.5 | – | 3 | – | ns | |
| Clock Low Pulse Width | t_{CL} | | 2.5 | – | 2.5 | – | 3 | – | ns | |
| Transition time | t_T | | 0.3 | 1.2 | 0.3 | 1.2 | 0.5 | 2 | ns | |

Setup and Hold Parameters

| | | | | | | | | | | |
|---------------------------------|-----------|--|-----|---|-----|---|---|---|-----|---|
| Input Setup Time | t_{IS} | | 1.5 | – | 1.5 | – | 2 | – | ns | 4 |
| Input Hold Time | t_{IH} | | 0.8 | – | 0.8 | – | 1 | – | ns | 4 |
| Power Down Mode Entry time | t_{SB} | | – | 1 | – | 1 | – | 1 | CLK | 4 |
| Power Down Mode Exit Setup Time | t_{PDE} | | 1 | – | 1 | – | 1 | – | CLK | 4 |
| Mode Register Set-up time | t_{RSC} | | 2 | – | 2 | – | 2 | – | CLK | |

Common Parameters

| | | | | | | | | | | |
|---|-----------|--|----|------|----|------|----|------|-----|---|
| Row to Column Delay Time | t_{RCD} | | 15 | – | 20 | – | 20 | – | ns | 5 |
| Row Precharge Time | t_{RP} | | 15 | – | 20 | – | 20 | – | ns | 5 |
| Row Active Time | t_{RAS} | | 42 | 100k | 45 | 100k | 50 | 100k | ns | 5 |
| Row Cycle Time | t_{RC} | | 60 | – | 67 | – | 70 | – | ns | 5 |
| Activate(a) to Activate(b) Command period | t_{RRD} | | 14 | – | 15 | – | 16 | – | ns | 5 |
| \overline{CAS} (a) to \overline{CAS} (b) Command period | t_{CCD} | | 1 | – | 1 | – | 1 | – | CLK | |

| Parameter | Symbol | Limit Values | | | | | | Unit |
|-----------|--------|-----------------|------|-------------------|------|-----------------|------|------|
| | | -7 PC133-222 | | -7.5 PC133-333 | | -8 PC100-222 | | |
| | | min. | max. | min. | max. | min. | max. | |

Refresh Cycle

| | | | | | | | | | |
|---------------------------------|------------|---|----|---|----|---|----|-----|---|
| Refresh Period (4096 cycles) | t_{REF} | – | 64 | – | 64 | – | 64 | ms | |
| Self Refresh Exit Time | t_{SREX} | 1 | – | 1 | – | 1 | – | CLK | 6 |

Read Cycle

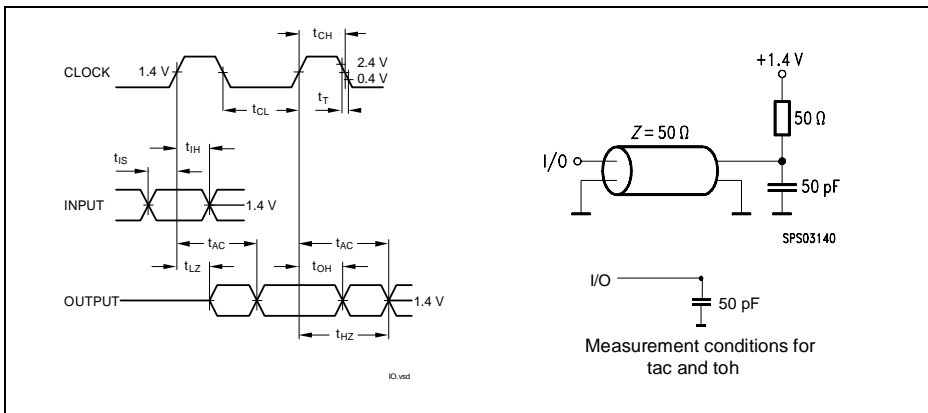
| | | | | | | | | | |
|---------------------------------|-----------|---|---|---|---|---|---|-----|---|
| Data Out Hold Time | t_{OH} | 3 | – | 3 | – | 3 | – | ns | |
| Data Out to Low Impedance Time | t_{LZ} | 0 | – | 0 | – | 0 | – | ns | |
| Data Out to High Impedance Time | t_{HZ} | 3 | 7 | 3 | 7 | 3 | 8 | ns | 7 |
| DQM Data Out Disable Latency | t_{DQZ} | – | 2 | – | 2 | – | 2 | CLK | |

Write Cycle

| | | | | | | | | | |
|---|-----------|---|---|---|---|---|---|-----|--|
| Data Input to Precharge (write recovery) | t_{WR} | 2 | – | 2 | – | 2 | – | CLK | |
| DQM Write Mask Latency | t_{DQW} | 0 | – | 0 | – | 0 | – | CLK | |

Notes:

- All AC characteristics shown are for SDRAM components.
 An initial pause of 100 μ s is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
- AC timing tests have $V_{il} = 0.4$ V and $V_{ih} = 2.4$ V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{ih} and V_{il} . All AC measurements assume $t_T = 1$ ns with the AC output load circuit shown. Specified t_{ac} and t_{oh} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0 V.



- If clock rising time is longer than 1 ns, a time ($t_T - 0.5$) ns has to be added to this parameter.
- If t_T is longer than 1 ns, a time ($t_T - 1$) ns has to be added to this parameter.
- Any time that the refresh period has been exceeded, a minimum of two Auto (CRB) Refresh commands must be given to "wake-up" the device.
- Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
- Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.

Serial Presence Detects:

A serial presence detect storage device - E²PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E²PROM device during module production using a serial presence detect protocol (I²C synchronous 2-wire bus)

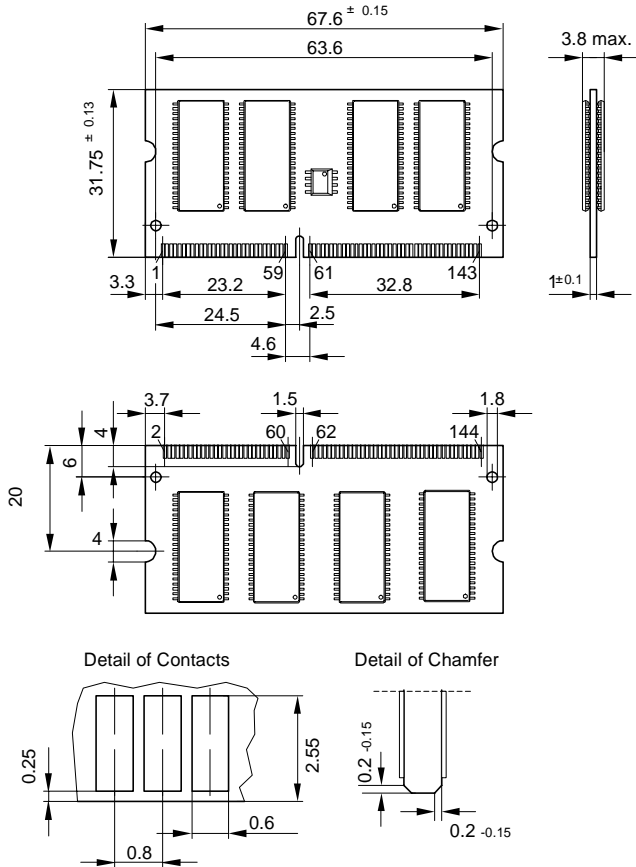
SPD-Table HYS64V16200GDL:

| Byte# | Description | SPD Entry Value | Hex | | |
|--------|--|-----------------------------|--------------|----------------|--------------|
| | | | 16Mx64 -7 | 16Mx64 -7.5 | 16Mx64 -8 |
| 0 | Number of SPD bytes | 128 | 80 | | |
| 1 | Total bytes in Serial PD | 256 | 08 | | |
| 2 | Memory Type | SDRAM | 04 | | |
| 3 | Number of Row Addresses | 13 | 0D | | |
| 4 | Number of Column Addresses | 9 | 09 | | |
| 5 | Number of DIMM Banks | 1 | 01 | | |
| 6 | Module Data Width | 64 | 40 | | |
| 7 | Module Data Width (cont'd) | 0 | 00 | | |
| 8 | Module Interface Levels | LVTTL | 01 | | |
| 9 | SDRAM Cycle Time at CL=3 | 7.5 / 10.0 ns | 75 | 75 | A0 |
| 10 | SDRAM Access time from Clock at CL=3 | 5.4 / 6.0 ns | 54 | 54 | 60 |
| 11 | Dimm Config (Error Det/Corr.) | none | 00 | | |
| 12 | Refresh Rate/Type | Self-Refresh, 7.8 μ s | 82 | | |
| 13 | SDRAM width, Primary | x16 | 10 | | |
| 14 | Error Checking SDRAM data width | n/a | 00 | | |
| 15 | Minimum clock delay for back-to-back random column address | $t_{cod} = 1$ CLK | 01 | | |
| 16 | Burst Length supported | 1, 2, 4 & 8 | 0F | | |
| 17 | Number of SDRAM banks | 2 | 04 | | |
| 18 | Supported CAS Latencies | 2, & 3 | 06 | | |
| 19 | CS Latencies | CS latency = 0 | 01 | | |
| 20 | WE Latencies | Write latency = 0 | 01 | | |
| 21 | SDRAM DIMM module attributes | unbuffered | 00 | | |
| 22 | SDRAM Device Attributes :General | V _{cc} tol +/- 10% | 0E | | |
| 23 | SDRAM Cycle Time at CL = 2 | 7.5 / 10 ns | 75 | A0 | |
| 24 | SDRAM Access Time from Clock at CL=2 | 5.4 / 6.0 ns | 54 | 60 | |
| 25 | SDRAM Cycle Time at CL = 1 | not supported | 00 | FF | |
| 26 | SDRAM Access Time from Clock at CL=1 | not supported | 00 | FF | |
| 27 | Minimum Row Precharge Time | 20 ns | 0F | 14 | |
| 28 | Minimum Row Active to Row Active delay | 15 / 16 ns | 0E | 0F | 10 |
| 29 | Minimum RAS to CAS delay | 20 ns | 0F | 14 | |
| 30 | Minimum Ras pulse width | 42 / 45 / 60 ns | 2A | 2D | 32 |
| 31 | Module Bank Density (per bank) | 128MB | 20 | | |
| 32 | SDRAM input setup time | 1.5 / 2 ns | 15 | 15 | 20 |
| 33 | SDRAM input hold time | 0.8 / 1 ns | 08 | 08 | 10 |
| 34 | SDRAM data input setup time | 1.5 / 2 ns | 15 | 15 | 20 |
| 35 | SDRAM data input hold time | 0.8 / 1 ns | 08 | 08 | 10 |
| 36-61 | Superset information | | 00 | FF | |
| 62 | SPD Revision | Revision 1.2 | 12 | | |
| 63 | Checksum for bytes 0 - 62 | | F4 | 39 | 9C |
| 64-125 | Manufactures's information | | | | |
| 126 | Frequency Specification | | 64 | | |
| 127 | Details | | 87 | | |
| 128+ | Unused storage locations | | FF | | |

SPD-Table HYS64V32220GDL:

| Byte# | Description | SPD Entry Value | Hex | | |
|--------|--|-----------------------------|--------------|----------------|--------------|
| | | | 32Mx64 -7 | 32Mx64 -7.5 | 32Mx64 -8 |
| 0 | Number of SPD bytes | 128 | 80 | | |
| 1 | Total bytes in Serial PD | 256 | 08 | | |
| 2 | Memory Type | SDRAM | 04 | | |
| 3 | Number of Row Addresses | 13 | 0D | | |
| 4 | Number of Column Addresses | 9 | 09 | | |
| 5 | Number of DIMM Banks | 2 | 02 | | |
| 6 | Module Data Width | 64 | 40 | | |
| 7 | Module Data Width (cont'd) | 0 | 00 | | |
| 8 | Module Interface Levels | LVTTL | 01 | | |
| 9 | SDRAM Cycle Time at CL=3 | 7.5 / 10.0 ns | 75 | 75 | A0 |
| 10 | SDRAM Access time from Clock at CL=3 | 5.4 / 6.0 ns | 54 | 54 | 60 |
| 11 | Dimm Config (Error Det/Corr.) | none | 00 | | |
| 12 | Refresh Rate/Type | Self-Refresh, 7.8 μ s | 82 | | |
| 13 | SDRAM width, Primary | x16 | 10 | | |
| 14 | Error Checking SDRAM data width | n/a | 00 | | |
| 15 | Minimum clock delay for back-to-back random column address | $t_{cod} = 1$ CLK | 01 | | |
| 16 | Burst Length supported | 1, 2, 4 & 8 | 0F | | |
| 17 | Number of SDRAM banks | 2 | 04 | | |
| 18 | Supported CAS Latencies | 2, & 3 | 06 | | |
| 19 | CS Latencies | CS latency = 0 | 01 | | |
| 20 | WE Latencies | Write latency = 0 | 01 | | |
| 21 | SDRAM DIMM module attributes | unbuffered | 00 | | |
| 22 | SDRAM Device Attributes :General | V _{cc} tol +/- 10% | 0E | | |
| 23 | SDRAM Cycle Time at CL = 2 | 7.5 / 10 ns | 75 | A0 | |
| 24 | SDRAM Access Time from Clock at CL=2 | 5.4 / 6.0 ns | 54 | 60 | |
| 25 | SDRAM Cycle Time at CL = 1 | not supported | 00 | FF | |
| 26 | SDRAM Access Time from Clock at CL=1 | not supported | 00 | FF | |
| 27 | Minimum Row Precharge Time | 20 ns | 0F | 14 | |
| 28 | Minimum Row Active to Row Active delay | 15 / 16 ns | 0E | 0F | 10 |
| 29 | Minimum RAS to CAS delay | 20 ns | 0F | 14 | |
| 30 | Minimum Ras pulse width | 42 / 45 / 60 ns | 2A | 2D | 32 |
| 31 | Module Bank Density (per bank) | 128MB | 20 | | |
| 32 | SDRAM input setup time | 1.5 / 2 ns | 15 | 15 | 20 |
| 33 | SDRAM input hold time | 0.8 / 1 ns | 08 | 08 | 10 |
| 34 | SDRAM data input setup time | 1.5 / 2 ns | 15 | 15 | 20 |
| 35 | SDRAM data input hold time | 0.8 / 1 ns | 08 | 08 | 10 |
| 36-61 | Superset information | | 00 | FF | |
| 62 | SPD Revision | Revision 1.2 | 12 | | |
| 63 | Checksum for bytes 0 - 62 | | F5 | 1E | 81 |
| 64-125 | Manufactures's information | | | | |
| 126 | Frequency Specification | | 64 | | |
| 127 | Details | | C7 | | |
| 128+ | Unused storage locations | | FF | | |

256 MByte SO-DIMM Module package (JEDEC MO-190)
(144 pin, dual read-out, single in-line memory module)



L-DIM-144-9

note: all tolerances are in accordance with the JEDEC standard

Change List

| | |
|------------|--|
| 6.99 | First and preliminary version, -8A only |
| 19.1.2000 | -7.5 and -8 speed sorts added |
| 19.7.2000 | CKE1 added to the block diagram |
| 24.7.2000 | GDL versions added for 256Mbit S17-C2 with 1.5mA ICC6 per component |
| 25.7.2000 | -8A speed sort removed backward compatibility for "C2" base modules clarified |
| 5.9.2000 | ICC6 changed from 6mA to 6.8 mA per memory bank after the component datasheet for 256M S17 changed from 1.5 to 1.7 mA ICC2PS changed from 16 to 8 mA |
| 24.11.2000 | ICC6 changed from 6.8 to 7.2 mA (Request from Axel Hahn and Uwe Fritsch) Component datasheet unchanged at ICC6=1.7mA Preliminary Capacitance Values added |
| 15.12.2000 | All reference to older versions based on 256M S20 removed |
| 5.3.2001 | ICC currents, where wrong and have been corrected according to the latest 256M S17 datasheet |
| 9.07.2001 | HYS64V16200GL-7/-7.5 and -8 added HYS64V1632220GDL-7 added |
| 6.09.2001 | SCR : Absolute Maximum Ratings Table added |



HYS64V16200GDL/HYS64V32220GDL
144 pin SO-DIMM SDRAM Modules
